Claims

What is claimed is:

1. A method of phase splitting for generating multi-phase clocks having the same frequency and predetermined phase differences between one another, comprising:

   generating multi-phase reference clocks having the same frequency higher than an output clock frequency and a multiple of the output clock frequency, the reference clocks having a predetermined reference phase difference between one another; and

   generating output clocks wherein periods of each output clocks are triggered by the corresponding reference periods apart from other reference periods by at least one or a plurality of periods of the reference clock.

2. The method of claim 1 wherein the frequency of the reference clocks is a multiple of the output clocks.

3. The method of claim 1 wherein the reference phase difference is plural times as high as an output phase difference, wherein the ratio of the reference phase difference is the same as the reference clocks and the output clocks.

4. The method of claim 1 wherein when the frequency of the reference clocks is N times as high as the output clocks, the method triggering periods of the corresponding output clocks according to the plurality of reference periods at intervals of at least (N-1) period.

5. The method of claim 1 wherein if two reference clocks have the reference phase difference of 360 degrees, the two reference clocks are essentially the same, and when using the two reference clocks to generate the corresponding two output clocks, the two output clocks are triggered by different reference periods of one reference clock.

6. The method of claim 1 wherein the two reference clocks are a first reference clock and a second reference clock, the method further comprising:

determining a first reference period of the first reference clock and also finding a second reference period in the second reference clock, lagging the first reference period;

dividing the frequency of the first reference clock at a time point corresponding to the first reference period in order to generate an output clock; and

dividing the frequency of the second reference clock at a time point corresponding to the second reference period in order to generate another output clock.

7. The method of claim 6 wherein the first reference clock leads the second reference clock by the reference phase difference.

8. The method of claim 1 wherein the periods of each output clock are triggered by the reference periods of the corresponding reference clock apart from other reference clocks by at least one or a plurality of periods of the reference clock wherein if a first period of an output clock is triggered by the first reference period of a corresponding reference clock, a second period of the output clock would be triggered by the reference period lagging the first reference period by the predetermined phase difference in the second reference clock, the second period of the output lagged the first period by the determined phase difference.

9. The method of claim 1 wherein the two reference clocks are a first reference clock and a second reference clock, the method further comprising:

selecting a first reference period in the first reference clock;

in the second reference clock, stopping the reference period from lagging the first reference period to generate an intermediate clock so that each reference period of the intermediate clock will lag the first reference period in the first reference clock; and

dividing the frequency of the first reference clock and the corresponding intermediate clock to generate two corresponding output clocks.

10. A multi-phase clock-generating circuit for generating two output clocks of the same frequency with a predetermined phase difference between each other,

comprising:

a clock generator for generating two reference clocks having the same frequency higher than and a multiple of the frequency of a corresponding output clock, the reference clocks having a predetermined reference phase difference between each other; and

a phase interpolator for generating two corresponding output clocks wherein each period of these two output clocks is triggered by the corresponding reference period, which is apart from other reference periods by at least one or a plurality of periods of the reference clock.

11. The multi-phase clock-generating circuit of claim 10 wherein the two reference clocks are a first reference clock and a second reference clock, the multi-phase clock-generating circuit further comprising:

a sequence triggering module for stopping the reference period of the second reference clock from lagging the first reference period to generate an intermediate clock; and

a frequency division module for dividing the frequency of the first reference clock and the corresponding intermediate clock to generate two corresponding output clocks; wherein each reference period of the intermediate clock lags the first reference period in the first reference clock

12. The multi-phase clock-generating circuit of claim 11 wherein the first reference clock leads the second reference clock by the reference phase difference.

13. The multi-phase clock-generating circuit of claim 10 wherein the two reference clocks are a first reference clock and a second reference clock, and the phase interpolator comprises:

a sequence triggering module for finding in the second reference clock a second reference period lagging the first reference period of the first reference clock, and producing a corresponding reset signal at the time corresponding to the second reference period;

a first frequency divider for generating an output clock by dividing the frequency of the first reference clock; and

a second frequency divider for generating the other output clock by dividing the frequency of the second reference clock after receiving the reset signal.

14. The multi-phase clock-generating circuit of claim 13 wherein the first frequency divider and the second frequency divider are triggered by rising edges.

15. The multi-phase clock-generating circuit of claim 10 wherein the frequency of the reference clocks is a multiple of the frequency of the output clocks.

16. The multi-phase clock-generating circuit of claim 10 wherein the reference phase difference is plural times as high as the output phase difference, and the ratio of the reference phase difference is the same as the ratio of the frequency of the reference clocks and the frequency of the output clocks.

17. A method of phase-splitting for generating two output clocks of the same frequency with a predetermined phase difference between each other, comprising:

generating a reference clock having a frequency higher than and a multiple of a frequency of a corresponding output clock, and substantially equal an integer multiple of a reference period; and

triggering periods of the different output clocks by the reference periods of the corresponding reference clocks to generate the two output clocks.

18. The method of claim 17 wherein the phase difference of the output clocks is not essentially equal to 360 degrees.

19. The method of claim 17 wherein the phase difference of the output clocks is not essentially equal to 180 degrees.

20. The method of claim 17 wherein if the frequency of the reference clock is N times as high as that of the output clock, the phase difference of the output clocks is a multiple of 360/N degrees.

21. The method of claim 17 wherein the frequency division is triggered by the first

reference period of the reference clock to generate an output clock, the second reference period lagging the first period of the reference clock starting frequency division to generate another output clock.

22. The method of claim 17 wherein a third output clock can be produced, output clock having the same frequency as the two output clocks but different phase, the method further comprising:

generating a second reference clock having the same clock frequency but a different reference phase as the reference clock; and

triggering each period of the third output clock according to each period of the second reference clock.